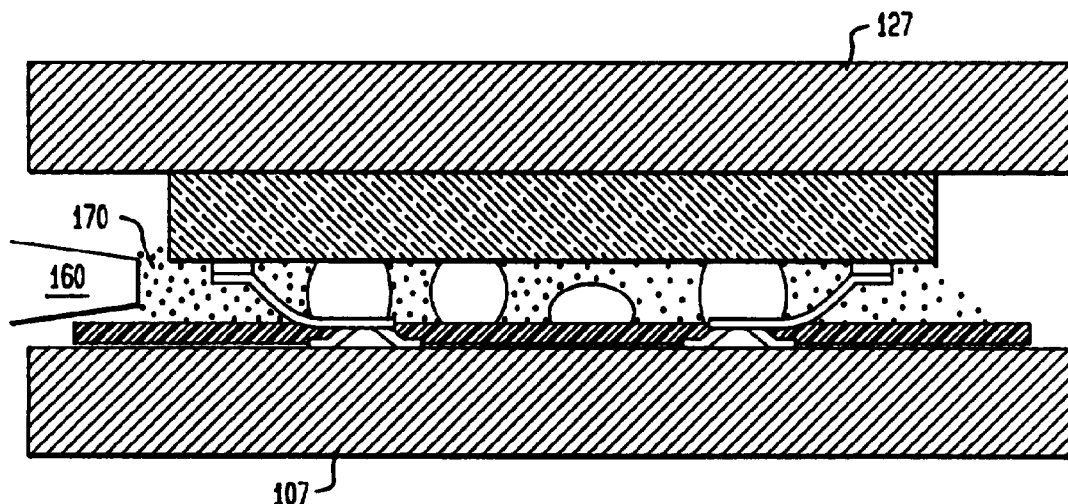




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<b>(21) International Application Number:</b> PCT/US95/11933 <b>(22) International Filing Date:</b> 20 September 1995 (20.09.95)  <b>(30) Priority Data:</b> 08/309,433           20 September 1994 (20.09.94)   US 08/365,699           29 December 1994 (29.12.94)   US  <b>(71) Applicant:</b> TESSERA, INC. [US/US]; 3099 Orchard Drive, San Jose, CA 95134 (US).  <b>(72) Inventors:</b> KOVAC, Zlata; 108 Wollin Way, Los Gatos, CA 95032 (US). MITCHELL, Craig; 530 Mansion Court #114, Santa Clara, CA 95054 (US). DISTEFANO, Thomas; 15363 Robin Ann Lane, Monte Sereno, CA 95030 (US).  <b>(74) Agents:</b> MILLET, Marcus, J. et al.; Lerner, David, Littenberg, Krumholz & Mentlik, 600 South Avenue West, Westfield, NJ 07090 (US).		<b>(81) Designated States:</b> AU, CA, CN, FI, JP, KR, MX, RU, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Published</b> <i>With international search report.</i> <i>Before the expiration of the time limit for amending the</i> <i>claims and to be republished in the event of the receipt of</i> <i>amendments.</i>

**(54) Title:** COMPLIANT INTERFACE FOR A SEMICONDUCTOR CHIP**(57) Abstract**

A method and an apparatus for providing a planar and compliant interface between a semiconductor chip (120) and its supporting substrate to accommodate for the thermal coefficient of expansion mismatch therebetween. The compliant interface is comprised of a plurality of compliant pads (110) defining channels (117) between adjacent pads. The pads are typically compressed between a flexible film chip carrier (100) and the chip. A compliant filler (170) is further disposed within the channels to form a uniform encapsulation layer having a controlled thickness.

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DESCRIPTIONCOMPLIANT INTERFACE FOR A SEMICONDUCTOR CHIPTechnical Field

The present invention relates, generally, to providing a compliant interface for a semiconductor chip, and more particularly relates to a method and apparatus for providing a compliant interface to accommodate for differences in the thermal coefficient of expansion mismatch between a semiconductor chip and a support structure, such as a printed wiring board.

Background Art

In attempting to use the area on printed wiring boards more efficiently, semiconductor chip manufacturers have recently been switching from larger, more cumbersome interconnection conventions, such as pin grid arrays ("PGAs") and the perimeter leaded quad flat packs ("QFPs"), to smaller conventions, such as ball grid arrays ("BGAs"). Using BGA technology, semiconductor chips are typically interconnected to their supporting substrates using solder connections, such as with "flip-chip" technology. However, when solder alone is used to interconnect the chip contacts to the substrate, the columns of solder are generally designed to be short to maintain the solder's structural integrity. This results in minimal elastic solder connection properties which further results in increased susceptibility to solder cracking due to the mechanical stress of the differential thermal coefficient of expansion ("TCE") of the chip relative to the supporting substrate thereby reducing the reliability of the solder connection. In other words, when the chip heats up during use, both the chip and the substrate expand; and when the heat is removed, both the chip and the substrate contract. The problem that arises is that the chip and the substrate expand and contract at different rates and at different times, thereby stressing the interconnections between them. As the features of semiconductor chips continue to be reduced in size, the

number of chips packed into a given area will be greater and the heat dissipated by the each of these chips will have a greater effect on the thermal mismatch problem. This further increases the need for a highly compliant  
5 interconnection scheme for the chips.

The solder cracking problem is exacerbated when more than one semiconductor chip is mounted in a package, such as in a multichip module. Multi-chip modules continue to grow in popularity; however, as more  
10 chips are packaged together, more heat will be dissipated by each package which, in turn, means the interconnections between a package and its supporting substrate will encounter greater mechanical stress due to thermal cycling. Further, as more chips are  
15 integrated into multichip modules, each package requires additional interconnections thereby increasing the overall rigidity of the connection between the module and its supporting substrate.

An interconnection solution put forth in U.S. Patent No. 4,642,889, entitled "Compliant  
20 Interconnection and Method Therefor" issued to Grabbe seeks to alleviate the aforementioned solder cracking problem by embedding wires within each solder column to reinforce the solder thereby allowing higher solder  
25 pedestals and more elasticity. Another solution includes spirally wrapping wire around the outside of the solder. A further solution put forth includes providing a combination of solder and high lead solder, as found in U.S. Patent No. 5,316,788, entitled  
30 "Applying Solder to High Density Substrates" issued to Dibble et al.

Still other prior art solutions make use of a underfill material disposed between the chip and the supporting substrate in an attempt to reduce the stress  
35 caused by TCE mismatch. Without the underfill material, this stress is typically concentrated at the weakest part of the solder balls. The underfill material allows this stress to be more uniformly spread out over the

entire surface of the solder balls. Examples of the use of underfill materials may be found in U.S. Patent Nos. 5,194,930, 5,203,076 and 5,249,101. All of these prior art solutions are aimed at reducing the shear stress  
5 endured by the interconnections caused by thermal cycling. However, each of these solutions also encounters significant problems such as insufficient compliancy and process cost.

Several inventions, commonly assigned to the  
10 assignee of the present invention, deal effectively, but specifically differently, with the thermal cycling problem. For example, U.S. Patent No. 5,148,266 discloses improvements in semiconductor chip assemblies and methods of making the same. As set forth in the  
15 '266 patent, a semiconductor chip can be connected to a substrate using a sheet-like, and preferably flexible, interposer. The interposer overlies the top, contact-bearing surface of the chip. A first surface of the interposer faces towards the chip whereas a second  
20 surface faces away from the chip. Electrical terminals are provided on the second surface of the interposer, and the interposer is provided with apertures extending through it. Flexible leads extend through these apertures between contacts on the chip and the terminals  
25 on the second surface of the interposer. The terminals can be bonded to a substrate. Because the terminals are movable relative to the contacts on the chip, the arrangements described in the '266 patent provide excellent resistance to differential expansion of the  
30 chip relative to the substrate caused by thermal cycling. The interposer disclosed in the '266 patent may also include a compliant layer disposed between the terminals and the chip.

Copending, commonly assigned United States  
35 Patent Application No. 08/123,882, filed September 20, 1993, discloses a method for creating an interface between a chip and chip carrier including spacing the chip a given distance above the chip carrier, and

introducing a liquid in the gap between the chip and carrier. Preferably, the liquid is an elastomer which is cured into a resilient layer after its introduction into the gap. In another preferred embodiment, the  
5 terminals on a chip carrier are planarized or otherwise vertically positioned by deforming the terminals into set vertical locations with a plate, and a liquid is then cured between the chip carrier and chip.

Despite the positive results of the  
10 aforementioned commonly owned inventions, still further improvements would be desirable.

#### Disclosure of Invention

The present invention provides a method and apparatus for providing a compliant interface for  
15 semiconductor chips to accommodate for the typically large thermal expansion mismatch between a chip and its support structure.

More specifically, one aspect of the present invention provides a method of fabricating a compliant  
20 interface for a semiconductor chip, typically comprised of a compliant encapsulation layer having a controlled thickness. A first support structure, such as a flexible, substantially inextensible dielectric film, having a surface is provided. A plurality of compliant  
25 pads are attached to the first surface of the first support structure, any two adjacent compliant pads defining a channel therebetween. Attaching the compliant pads to the first support structure may be accomplished a number of different ways. In one  
30 embodiment, a stencil mask having a plurality of holes extending therethrough is placed on top of the first surface of the support structure. The holes in the mask are then filled with a curable liquid elastomer. Desirably, liquid elastomer has a thick enough  
35 consistency so that the mask may then be removed before curing the elastomer. After the mask has been removed, the elastomer is at least partially cured, such as by heating or exposing to ultra-violet light. The filling

step may be accomplished by screening the liquid elastomer across an exposed surface of the mask such that the elastomer is deposited into the holes of the mask. Other methods are also suitable, such as  
5 dispensing the elastomer into each of the holes individually. Thus, there is provided an assembly which includes an array of compliant pads further having channels between substantially all of the adjacent pads.

At this stage of the process, the vertical height of  
10 the pads need not be extremely uniform.

In a further stage, the assembly including the array of pads is used with a second support structure. In one embodiment, the second support structure is a semiconductor chip having a plurality of contacts on a  
15 first surface. The first surface of the chip is abutted against the array of compliant pads and the contacts are electrically connected to a corresponding plurality of terminals on a second side of the support structure. Typically, the first surface of the chip is pressed  
20 against the pads to compress them, thus ensuring the chip is uniformly supported across its first surface and further ensuring the planarity of the first support structure, or flexible dielectric film, with respect to the first surface of the chip. Where the dielectric  
25 film has terminals thereon, the terminals desirably are held coplanar with one another during this step. For example, the dielectric film and the chip may be held between a pair of opposed platens, so that the terminals bear on one platen and are brought into a substantially  
30 coplanar condition. A compliant filler, such as a curable liquid elastomer, is then injected into the channels between the chip and the support structure and around the compliant pads while the chip and support structure are held in place. The elastomer may then be  
35 cured to form a substantially uniform, planar, compliant layer between the chip and the support structure.

In a further embodiment, the second support structure includes a plurality of chips. The array of

compliant pads is large enough to overly several chips simultaneously. This method may be used to form a compliant interface for multiple chips which then may either be cut into individual chips or may be used as a multi-chip module. The above method may also be used to form a compliant interface for a semiconductor wafer before the individual chips are separated. After the compliant interface is formed, the wafer may be cut into individual chips or into multi-chip modules.

A further embodiment provides for an array of compliant pads held in place using a holding element. The pads are then fixably placed to either a surface of the chip or the supporting substrate. The holding element is then removed and the pads are compressed between the chip and the supporting substrate. Liquid elastomer is injected into the channels between the adjacent pads, as described in the above embodiments.

The pads or the pad/injected elastomer combination provide a compliant, planar interface which effectively accommodates for the thermal coefficient of expansion mismatch between the chip and a supporting substrate thereby alleviating much of the stress on the connections therebetween. Further, the combination provides an effective encapsulation barrier against moisture and contaminants.

The foregoing and other objects and advantages of the present invention will be better understood from the following Detailed Description of a Preferred Embodiment, taken together with the attached Figures.

#### Brief Description of the Drawings

Figure 1 shows a side view of one embodiment of a compliant semiconductor chip interface having a plurality of compliant pads, according to the present invention.

Figure 2 shows a side view of the embodiment shown in Figure 1, wherein the channels between the compliant pads are filled with a curable liquid, according to the present invention.



Figures 3A and 3B show a side view of the mask and elastomer used to form the compliant pads, according to further embodiments of the invention.

Figures 4A-C show a top plan view of several  
5 different pad shapes and registrations in relation to the terminal's positions, according to further embodiments of the invention.

Figures 5A and 5B show a perspective and a side view of the support structure and compliant pads,  
10 according to a further embodiment of the present invention.

Figure 5C shows a side view of the embodiment shown in Figures 5A and 5B, wherein multiple encapsulated chips have been abutted against the  
15 compliant pads.

Figure 6 shows a side view of a compliant interface being formed between a wafer and the support structure, according to a further embodiment of the present invention.

Figure 7 shows a side view of a plurality of compliant pads disposed within holes in a holding element, according to a further embodiment of the present invention.

Figure 8 shows a side view of a further  
25 embodiment of the invention having a compliant interface between a heat spreader and a support structure.

#### Modes for Carrying Out the Invention

Figures 1 and 2 show a side view of a chip size package embodiment, according to the present  
30 invention. A support structure 100 is provided having a first and a second surface. The support structure 100 may be substantially rigid, semi-rigid or flexible. However typically, the support structure 100 is comprised of a flexible, but substantially inextensible,  
35 dielectric film, preferably formed from a polymeric material, such as Kapton™ "E" available from DuPont Chemical Corp., of an approximate thickness between 25 microns and 75 microns. Further, the dielectric film

100 typically has conductive terminals 140 on its second surface.

A plurality of dielectric compliant pads 110 are attached to the first surface of the film 100. The compliant pads 110 are typically made of an curable liquid elastomer material, such as the Dow Corning silicone elastomer 577, known as "Sylgard™", with about 5-10% of fumed silica in order to obtain a stiff, thixotropic consistency. The height of the compliant pads 110 is nominally uniform, as defined by the measurement from the base of the pads, at the first surface of the film, to the apexes of the pads. However, exact uniformity in height is not critical, as discussed below. The ratio of width to height of each pad 110 is desirably about two to one (2:1) or greater in order to maintain good pad structural integrity. Each pad desirably has width or diameter, measured at its juncture with first surface of the film 100, between about 300  $\mu\text{m}$  to 2000  $\mu\text{m}$ . The pads are arranged in a grid pattern with center-to-center distance or "pitch" greater than the minimum width of each pad and preferably greater than the maximum width of each pad. Thus, each pair of mutually adjacent pads defines a channel 117 between them, and all of the channels are interconnected with one another to define a substantially continuous grid of channels 117. The pad pitch and hence the width of the channels 117 must be large enough to allow a compliant filler material 170 to be injected into the channels 117, as described in greater detail below.

As shown in Figure 3A and 3B, the compliant pads 110 are typically formed and attached to the dielectric film 100 using a stencil mask 80 having top and bottom surfaces and further having a plurality of holes 90 extending therethrough. In a preferred embodiment, the bottom surface of the mask 80 is placed atop the first surface of the film 100 and curable liquid elastomer is wiped or screened across the first

surface of the mask 80 so that the elastomer is deposited into each of the holes 90. If the elastomer is viscous or thixotropic enough, the mask is then typically removed and the pads are cured or partially  
5 cured by heating or exposing them to ultra-violet light or a combination thereof, such as by exposing the elastomer to ultraviolet light to create a "skin" of cured elastomer and then curing or partially curing the elastomer by a heating step. In the case of Dow 577  
10 elastomer, the elastomer is typically heated to approximately 125° C for 40 minutes. The mask 80 may also be removed after the curing step. In this case, the elastomer will conform to the shape of the hole 90 in the mask as it begins to cure. Thus, the  
15 pads 110 in Figure 3A will be cylindrical in shape with substantially flat top surfaces. If the mask 80 is left atop the dielectric film 100 during the curing step, the pads may partially adhere to the mask 80 at an exposed top edge of each hole 90 on the first surface of the  
20 mask as the elastomer cures. This makes removal of the mask 80 while maintaining the integrity of the pads 110 difficult. This problem can be effectively dealt with by using an alternate stencil mask 85, shown in Figure 3B, where each hole in the mask has a smaller top edge  
25 circumference on the top surface of the mask 85 than on the bottom surface of the mask 85. The smaller circumference of each hole reduces the strength of the attachment of the compliant pads 110 to the mask 85. However, because of the shape of enclosure 95 of the  
30 embodiment shown in Figure 3B, the liquid elastomer typically must be screened across the first surface of the mask in two directions to ensure the enclosure 95 is completely filled. The elastomer will then take on a rounded shape corresponding the shape of the enclosure  
35 95 and will retain its shape after curing. The Dow 577 elastomer, discussed above, also shrinks by approximately 5% during the curing step thereby facilitating the removal of the mask 85. Another

solution to this problem would be to coat the mask 80 with a material that will resist the adherence of the elastomer as it cures.

Returning to Figure 1, a semiconductor chip  
5 120 is next abutted to the compliant pads 110. The chip 120 has a face surface bearing contacts 130 and a back surface. The face surface of the chip is aligned with the compliant pads so that the none of the pads 110 cover the contacts on the chip. In the next step of the  
10 operation, the dielectric film 100 and the second support structure or chip 120 are squeezed together between a first platen 107 and a second platen 127. The platens are urged toward one another by a press (not shown). The first platen bears on the terminals 140 of  
15 the film 100, and forces these terminals into substantially coplanar alignment, whereas the second platen bears on the back surface of chip 120. During this process, the pads 110 are compressed. The extent of such compression varies from pad to pad, depending  
20 upon the original height of each pad, the heights of the various terminals 140 and other tolerances. Because the pads can accommodate variations in this manner, the heights of the pads prior to compression need not be precisely uniform. Some particularly short pads, such  
25 as pad 115, may not contact the chip surface even after compression. This situation is acceptable provided that the remaining pads substantially support the terminals 140 against the first platen.

Where the pads 110 are only partially cured  
30 during the pad forming process, described above, they are tacky and adhere to the chip 120 when it is compressed thereagainst. In a preferred embodiment, the chip 120 would be heated to about 100° to 180° C and then compressed against the pads 110 so that the  
35 partially cured pads 110 fully cure due to the heat of the chip 120 and in so doing adhere to the face surface of the chip. Alternately, the apex of each pad may be made tacky by providing an adhesive, a silicone gel, or

a film of uncured silicone elastomer thereon so that the chip 120 adheres thereto. Similarly, the chip surface may be coated with an adhesive in the regions remote from the contacts 130 so that the tips of the pads 110  
5 engage such adhesive. While adherence of the pads 110 to the chip 120 helps maintain the alignment between the chip 120 and the film 100, it is not imperative that the pads 110 are adhered to the chip 120 so long as the chip can be held in place by compressing it against the pads  
10 110. The heat and pressure applied during this step of the process permanently deform or "set" the pads to the heights and shapes achieved when the film and chip are squeezed between the platens. Once set in this manner, the pads tend to retain the film and chip in the same  
15 relative positions as achieved during the squeezing step, and thereby tend to retain the terminals 140 in coplanar alignment with one another.

The contacts 130 on the chip 120 are then attached to the terminals 140 on the film 100 through  
20 any suitable means. In this embodiment, each contact 130 is electrically connected to one terminal 140 through a flexible lead 150 extending therebetween. The terminal 140 is comprised of a conductive blind via (a via extending from the second to the first surface of  
25 the film 100 and having a closed bottom surface substantially in a plane with the first surface of the dielectric film 100) and a solder ball (shown in dashed lines), which is typically attached after the package is complete.

30 As shown in Figure 2, a low viscosity compliant filler 170 is then disposed between the chip 120 and the dielectric film 100 through the channels between the adjacent pads 110. An injection nozzle 160 is disposed adjacent an edge of the film 100. The  
35 filler 170 passes through the nozzle into the channels 117. The compliant filler 170 may be comprised of an elastomer, a gel or a compliant thixotropic material so long as the elastomer, gel or material retains its

compliance. One example of such a filler is Dow Corning elastomer Q1-4939. In a preferred embodiment, the filler 170 is comprised of a curable liquid elastomer having a viscosity adapted to facilitate flow of the liquid into the channels 117 between the adjacent pads 110. An evacuated environment can also be provided during the elastomer flow so that voids in the liquid elastomer caused by trapped air may be eliminated. Capillary action tends to pull the low viscosity liquid elastomer 170 into the channels 117 as the elastomer wets the pads, the chip and the film. The liquid elastomer 170 tends to remain between the chip and the substrate because of the surface tension forces. If necessary, however, the edges of the assembly may be closed by any suitable means to trap the liquid 170. During this process, the liquid elastomer also encapsulates leads 150. The liquid 170 is then cured, typically by heating the assembly while it is held between flat opposing surfaces, such as the platens 107, 127 used for the compression step. This results in a planar, compliant interface between the chip 120 and the dielectric film 100. The resulting assembly may then be freed to form an individual semiconductor chip package.

It is important to understand that the function of the compliant pads is to provide a uniformly supported, planar standoff between the chip and the dielectric film, while allowing the compliant filler to be injected between the adjacent pads 110 to create a compliant encapsulation layer having a controlled thickness. So long as there is uniformity of support, it does not matter whether the pads 110 are in direct registration with single or multiple terminals 140, as shown in Figures 4A and 4B, or whether the pads 110 are in random registration with respect to the terminals 140, as shown in Figure 4C. It also does not matter whether all of the pads in a common array are of the same general shape or dimension.

Figure 5A shows a top plan of a preferred embodiment of the first support structure and the compliant pads. Tape 200 is a continuous elongated strip of film with handling and locating features such as sprocket holes 210 adapted for engagement by tape-handling equipment of the type commonly employed in tape automated bonding or "TAB" processing in the semiconductor industry. Tape 200 includes a plurality of regions 201 spaced apart along its length, each such region constituting a support structure for one chip. Each region has pads 220 disposed in a grid on its first surface so that the pads define channels 203 therebetween, and has terminals 207 on its second surface, the terminals being connected to leads 225 extending across an aperture or "bond window" 215 in the tape, the bond window being in the form of a slot extending around a rectangular loop. The leads are adapted for bonding to the contacts of the chip. For example, each lead may have a detachable section as disclosed in International Patent Publication WO 94/03036, the disclosure of which is hereby incorporated by reference herein. The terminals and leads can be arranged in a "fan out" pattern, wherein the terminals are disposed on that portion of the tape outside of the loop defined by the bond window; in a "fan in" pattern wherein the terminals are disposed on that portion of the tape encircled by the bond window; or both. Such a tape can be mass-produced, to include numerous regions.

In use, a series of chips can be bonded to the various regions of the tape by abutting each chip against the compliant pads of one region and compressing and bonding the chip and pads in the same manner as discussed above. Each pad 220 may be only partially cured, or else may have a tacky layer 230 (Fig. 5B) of adhesive, silicone gel or uncured silicone elastomer on its apex, so that the pads will adhere to the chip. Alternatively or additionally, the chip may have such a tacky layer on its first surface in areas remote from

the contacts. During the abutting step, the tape is juxtaposed with each chip so that one region of the tape overlies the chip, and the contacts of each chip are brought into coarse alignment with the leads of the  
5 associated region of the tape, using conventional machine-vision alignment techniques. This alignment is maintained during the compressing and pad bonding steps.

After the pads have been bonded to the surfaces of the chip, the bonded pads maintain the alignment of the  
10 leads and contacts. The terminals of each region are electrically connected to the contacts of the associated chip, as by advancing a bonding tool into the bond window to engage each lead and connect it to the aligned contact of the chip.

15 Preferably, the bonding tool captures the bond region of the lead and brings it into more precise alignment with the chip contact. After bonding the leads, the compliant filler is introduced into the channels 203 between the pads, in substantially the same  
20 way as described above. Typically, the film 200 and the chip are compressed while the liquid material is introduced. These operations may be performed at separate stations of a processing line. At any time after the pads of a region have been bonded to a chip,  
25 the chip can be transported to the next station of the processing line by moving the tape using the sprocket holes 210. Each region of the tape can be severed from the remainder of the tape after all of the process steps have been completed to provide an individual chip and  
30 film assembly. Alternatively, each region can be severed before the final process step, and a portion of the process can be completed after severance. In a further embodiment of the invention, a plurality of individual regions of the tape may remain connected to  
35 one another,

Typically, each of these leads 225 will be detached within or near an edge of the bonding window 215 when such lead is connected to a respective chip



contact pad. If the leads and the terminals are arranged in a fan-out pattern, this action detaches the tape center portion 205, generally centered within the loop defined as the bonding window 215 from the outer portions of the tape. However, the compliant pads 220 disposed on the tape center portion 205 provides support for the leads 225 during the bonding phase. Conversely, in a fan-in arrangement, the exterior portion of each region may optionally be removed after connecting the leads.

In the alternative embodiment shown in Figure 5C, a plurality of individual regions 201 of the tape remain together and are not severed from one another during the process. A short length of tape thus retains a plurality of chips side-by-side, as a multi-chip module.

Thus, as illustrated in Fig. 5C, the back surfaces of these chips or modules may be mated to heat spreader/sinks 270 before or after the step of cutting the short length of tape bearing the chips free from the remainder of the tape. Further, a thermally conductive die attach material may be used between the chips 240 and the heat spreader 270 to aid in the transfer of heat from the chips. Such die attach materials are widely used in the semiconductor industry.

In a further alternative arrangement, a plurality of individual regions, each adapted to form a support structure for an individual chip, are formed side-by-side in a two-dimensional array on a unitary film in the shape of a panel. Plural chips are attached to these regions in the same manner as discussed above, so as to form a multichip assembly. In either arrangement where plural chips are employed, the steps of abutting and compressing the pads and injecting the liquid compliant filler can be performed simultaneously for all of the chips, using platens large enough to accommodate the entire array, or seriatim so that each chip is processed separately.

Figure 6 shows a side view of a compliant interface, as described in reference to Figures 1 and 2, being formed between a second support structure or semiconductor wafer 350 having contacts (not shown) on a first surface and a first support structure or film 300.

The wafer 350 includes an integral plurality of individual chips, each defining a portion of the first surface, and each including a plurality of contacts thereon. The film 300 has terminals 305 on its second surface, with leads (not shown) connected to the terminals 305. The terminals 305 and leads are disposed in a plurality of regions, each corresponding to one chip. Each region of the film may include a bond window (not shown), as discussed above.

Before engagement with the wafer 350, compliant pads 320 defining channels 325 therebetween are formed on the first surface of the film. Here again, each pad 320 may be only partially cured, or may have a curable tacky material on its apex. The film 300 is stretched taut and bonded to a rigid ring structure 310. The film 300 is then aligned with the wafer so that each region of the film is aligned with one chip of the wafer, and so that the leads are aligned with the contacts. The wafer is then abutted against the compliant pads 320. A platen 360 is applied on the back surface of the wafer 350. Another platen 370 is applied on the second surface of the film so as to engage the terminals 305. In the same manner as described above, the platens are forced toward one another, thereby compressing pads 320 and bringing the contacts 303 into substantially coplanar alignment with one another. While the contacts and pads are held in this position, the pads may be fully cured or set by heating the platen 360/wafer 350, thereby securing the film in position on the wafer. Alternately, a tacky adhesive may be applied to the first surface of the wafer around the contacts thereon to ensure the adherence of the pads 320 to the wafer 350. After this operation, the leads are bonded

to the wafer contacts, followed by injection of the liquid curable elastomer 340 into the channels 325. While the contacts are again held in position by the platens, the liquid elastomer is cured to form a  
5 complete assembly encompassing the entire wafer and all regions of the film.

Individual, fully encapsulated parts may then be cut from the wafer. These separated parts will have a compliant interface to accommodate for the thermal  
10 coefficient of expansion mismatch between the parts and their eventual supporting substrates, such as printed wiring boards. Further, the encapsulant protects the individual parts from moisture and contaminants.

Figure 7 shows a further embodiment having an  
15 array of compliant pads 410 held in place using a holding element 400. The pads 410 are then fixably placed atop either the contact bearing surface of a semiconductor chip (second support structure) or a flexible dielectric film (first support structure)  
20 typically by placing a tacky adhesive onto one of those surfaces. The holding element 400 is then removed. Desirably, the holding element 400 is made of a material which will break apart or peel off the pads easily so that the adherence of the pads 410 to either the wafer  
25 or the film is not comprised. The pads 110, as shown in Figure 1, are not typically screened across and cured to the contact bearing surface of the chip for fear that the contacts will be contaminated by stray uncured elastomer. In the embodiment shown in Figure 7,  
30 however, the pads are being attached after they have been either fully cured or partially cured to the point that they may retain their individual structural integrity. Thus, the pads 410 may be accurately placed and typically adhered on the chip's surface without any  
35 substantial fear that the chip's contacts will be contaminated. The pads are then compressed between the chip and the supporting substrate using platens and liquid elastomer is next injected into the channels

between the adjacent pads and cured, as described more fully in relation to the above embodiments.

The embodiment shown in Figure 8 shows a side view of an alternate embodiment in which the pads 510 are compressed between a second support structure which includes a heat spreader 520 having an indentation on its first side and a first support structure 500, which includes a flexible dielectric film. A chip 530 is disposed within the indentation of the heat spreader 520 so that the front or contact-bearing surface 580 of the chip faces outwardly at the opening of the indentation, and thus faces outwardly from the first surface 570 of the heat spreader. Dielectric film 500 has a bond window 550, terminals 590 on one surface and leads 595 connected to the terminals 590. After pads 510 are provided on the dielectric film 570 or the heat spreader by any of the techniques discussed above, the dielectric film 500 and the heat spreader 520 are aligned so that the outer portions of the dielectric film overlie the first surface 570, and so that the bond window 550 is aligned with the contacts on the chip. The leads 595 are bonded to the contacts of the chip. After bonding the leads, the bond window is closed by a sheet 540 of a further dielectric material such as a solder mask material which adheres to film 500 and thus forms a continuation of the film 500. Typically before bonding the leads, the pads 510 are compressed against first surface 570 by engaging the heat spreader 520 and the film 500 between a pair of platens (not shown) so that one such platen bears on the rear surface of the heat spreader, opposite from surface 570 and so that the other platen bears on terminals 590. This compression brings the terminals into coplanar alignment. As described above, the liquid compliant filler 560 is injected into the channels between the pads and cured while the platens hold the system in compression. In this embodiment, the pads are not provided at the interface between sheet 540 and the chip 530. If a

solder mask 540, or other suitable containing means, is placed over the bonding window 550, a compliant filler material 560 may be injected between the adjacent pads 510 creating a planar, compliant interface while  
5 simultaneously encapsulating the chip 530.

Having fully described several embodiments of the present invention, it will be apparent to those of ordinary skill in the art that numerous alternatives and equivalents exist which do not depart from the invention  
10 set forth above. It is therefore to be understood that the present invention is not to be limited by the foregoing description, but only by the appended claims.

#### Industrial Applicability

The invention can be employed for mounting  
15 semiconductor chips and other electronic components.

CLAIMS:

1. A method of fabricating a compliant interface for a semiconductor chip, comprising the steps of:

5           providing a first support structure (100) having a first surface and a porous resilient layer on the first surface of the first support structure;  
          abutting a first surface of a second support structure (120) against the porous layer; characterized  
10 by the step of

          disposing a first curable liquid (170) within the porous layer after the abutting step.

2. The method as claimed in claim 1, wherein the first liquid is a curable elastomer or a curable gel  
15 encapsulant.

3. The method as claimed in claim 1, further comprising the step of providing an evacuated environment prior to the disposing step.

4. The method as claimed in claim 1, wherein  
20 the porous, resilient layer includes a plurality of compliant pads (110), the pads defining channels therebetween, wherein the first curable liquid is disposed between the channels;

5. The method as claimed in claim 4, further  
25 characterized by the step of at least partially curing the first liquid after the first liquid has been introduced between the channels whereby a compliant layer is formed between the support structures.

6. The method as claimed in claim 5, further  
30 characterized by the step of compressing the compliant pads (110) between the first and second support structures (100, 120) prior to the disposing step.

7. The method as claimed in claim 6, wherein  
35 the compressing step includes the step of engaging the first and second support structure between a pair of opposed platens (107, 127) and urging the platens together.

8. The method as claimed in claim 7, further characterized in that the first support structure has a plurality of terminals (140) on a second surface remote from the second support structure and one of the platens  
5 (107) bears on the terminals (140) so as to bring the terminals into substantially coplanar alignment with one another before the disposing step.

9. The method as claimed in claim 8, wherein the compressing step includes the step of setting the  
10 compliant pads so that the pads tend to retain the terminals in said substantially coplanar alignment.

10. The method as claimed in claim 9, further characterized in that the first support structure is a flexible dielectric sheet.

15 11. The method as claimed in claim 1, further characterized in that the step of providing said first support structure includes the steps of:

providing a mask (80) having a plurality of holes therethrough atop the first surface of the support  
20 structure (100);

filling the holes in the mask with a second curable liquid;

removing the mask; and

at least partially curing the second liquid,  
25 whereby the compliant pads (110) are produced.

12. The method as claimed in claim 11, wherein the step of curing the second liquid includes the step of heating the second liquid to between 100° to 180° C.

30 13. The method as claimed in claim 11, wherein the step of curing the second liquid includes the step of exposing the second liquid to ultraviolet light.

14. The method as claimed in claim 11,  
35 wherein the step of curing the second liquid includes the steps of at least partially curing the second liquid using a combination of ultraviolet light and heat.

15. The method as claimed in claim 11, further characterized in that the filling step includes applying the second liquid across an exposed surface of the mask so that the second liquid fills the holes in the mask, and in that the holes (95) in the mask (85) have a smaller diameter at an exposed surface and a larger diameter at a surface adjacent the first surface of the dielectric sheet.

16. The method as claimed in claim 10, further characterized in that the second support structure (120) is a semiconductor chip having a plurality of contacts (130) on the first surface thereof.

17. The method as claimed in claim 16, further comprising the step of electrically connecting each contact (130) to one terminal (140) before the disposing step.

18. The method as claimed in claim 17, further characterized in that the abutting step further includes aligning the chip so that no compliant pad covers a contact.

19. The method as claimed in claim 18, further characterized by the step of heating the chip prior to compressing it against the compliant pads causing any partially cured pad to more fully cure and adhere to the chip.

20. The method as claimed in claim 10, further characterized in that the second support structure includes a heat spreader (520) having an indentation on a first side, the method further comprising disposing a semiconductor chip (530) having contacts on a first surface within the indentation such that the contacts face outwardly toward the first surface of the first support structure (540).

21. The method as claimed in claim 20, further characterized by the step of heating the heat spreader prior to compressing it against the compliant



pads causing any partially cured pad to more fully cure and adhere to the heat spreader.

22. The method as claimed in claim 26, further comprising the step of electrically connecting  
5 each contact to one terminal (540) prior to the disposing step.

23. The method as claimed in claim 10, further characterized by the step of adhering a second surface of the second support structure to a contact  
10 bearing surface of a semiconductor chip having contacts thereon.

24. The method as claimed in claim 24, further characterized in that the second support structure is a flexible dielectric sheet.

15 25. The method as claimed in claim 1, wherein the step of providing further includes the steps of:

providing a holding element (400) having a plurality of holes therethrough;

20 filling the holes in the holding element with a curable liquid elastomer;

curing the elastomer; and

adhering the elastomer to the first surface of the dielectric sheet after the curing step.

25 26. A method as claimed in claim 1 for fabricating a compliant interface for a plurality of semiconductor chips:

further characterized in that said first support structure has said first surface and a second surface, the second surface having a plurality of  
30 terminals (260) thereon, said providing step includes the step of attaching a plurality of compliant pads (220) to the first surface of the support structure, the pads defining channels therebetween, said second support structure including a plurality of separate  
35 semiconductor chips (240) each having a contact bearing surface and contacts on such surface, the chips being disposed in an array so that the contact bearing surfaces face in a common direction and define a first

chip surface, said abutting step including the step of abutting the first chip surface against the compliant pads, said disposing step including the step of disposing a liquid between the channels after the  
5 abutting step, whereby the semiconductor chips and the support structure define a single assembly, the method further including the step of electrically connecting each terminal to one contact.

27. The method as claimed in claim 26,  
10 further characterized by the step of curing the liquid after the liquid has been introduced between the channels whereby a compliant layer between the first chip surface and the support structure is formed.

28. The method as claimed in claim 27,  
15 further characterized by the step of subdividing the single assembly into individual parts each including at least one chip after the curing step.

29. The method as claimed in claim 28,  
further characterized in that the first support  
20 structure is a flexible dielectric sheet, and the abutting step includes compressing the compliant pads with the first chip surface.

30. A method as claimed in claim 1 further characterized in that said first support structure (300)  
25 has said first surface and a second surface, the second surface having a plurality of terminals (305) thereon;

said providing step includes the step of attaching a plurality of compliant pads (320) to the first surface of the support structure, the pads  
30 defining channels therebetween;

said second support structure is a wafer (350) having a plurality of integral semiconductor chips each having a plurality of contacts thereon, said abutting  
step including the step of abutting said wafer against  
35 the compliant pads;

the method further comprising the step of electrically connecting each contact to one terminal;  
and

said disposing step including the step of disposing said liquid between the channels after the electrically connecting step.

31. The method as claimed in claim 30,  
5 further characterized by the step of curing the liquid after the liquid has been introduced between the channels, whereby a compliant layer between the wafer and the support structure is formed.

32. The method as claimed in claim 31,  
10 further characterized by the step of subdividing the wafer into individual chips after the curing step.

33. The method as claimed in claim 31,  
further characterized in that the support structure is a flexible dielectric sheet, and wherein the abutting step  
15 includes compressing the compliant pads between the first surface of the wafer and the dielectric sheet prior to the disposing step.

34. A compliant interface for a semiconductor chip, comprising:

20 a first support structure (100) having a first surface;

a plurality of compliant pads (110) attached to the first surface of the support structure, the pads defining channels (117) therebetween;

25 a first surface of a second support structure (120) abutted against the compliant pads; and

a compliant filler disposed within the channels.

35. The interface as claimed in claim 34,  
30 further characterized in that the filler is a fully or partially curved elastomer or a gel encapsulant.

36. The interface as claimed in claim 34,  
further characterized in that the first support structure is a flexible dielectric sheet (100, 200)  
35 having a plurality of terminals (140, 207) on a second surface.

37. The interface as claimed in claim 36,  
further characterized in that the second support

structure is a semiconductor chip having a plurality of contacts on the first surface thereof.

38. The interface as claimed in claim 37, further comprising means for electrically connecting  
5 each contact on the chip to one terminal.

39. The interface as claimed in claim 36, further characterized in that the second support structure is a heat spreader (520) having a indentation on the first side, the heat spreader further including a  
10 semiconductor chip having contacts on a first surface disposed within the indentation such that the contacts face opposite the first surface of the first support structure.

40. The interface as claimed in claim 35,  
15 further characterized in that the second support structure is a flexible dielectric sheet (540) , a second surface of the second support structure being adhered to a contact bearing surface of a semiconductor chip having contacts thereon.

20 41. The interface as claimed in claim 35, further characterized in that the second support structure includes a plurality of separate semiconductor chips (240) each having a plurality of contacts on a contact bearing surface thereof, the chips being  
25 disposed in an array so that the contact bearing surfaces face in a common direction and define the first surface of the second support structure.

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FIG. 1

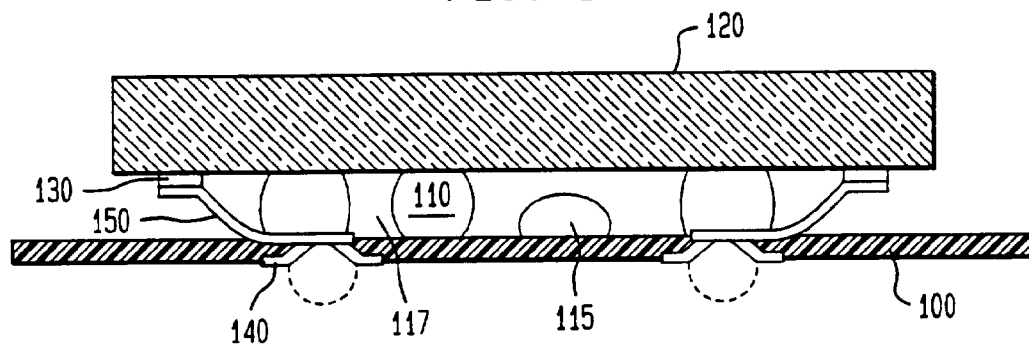
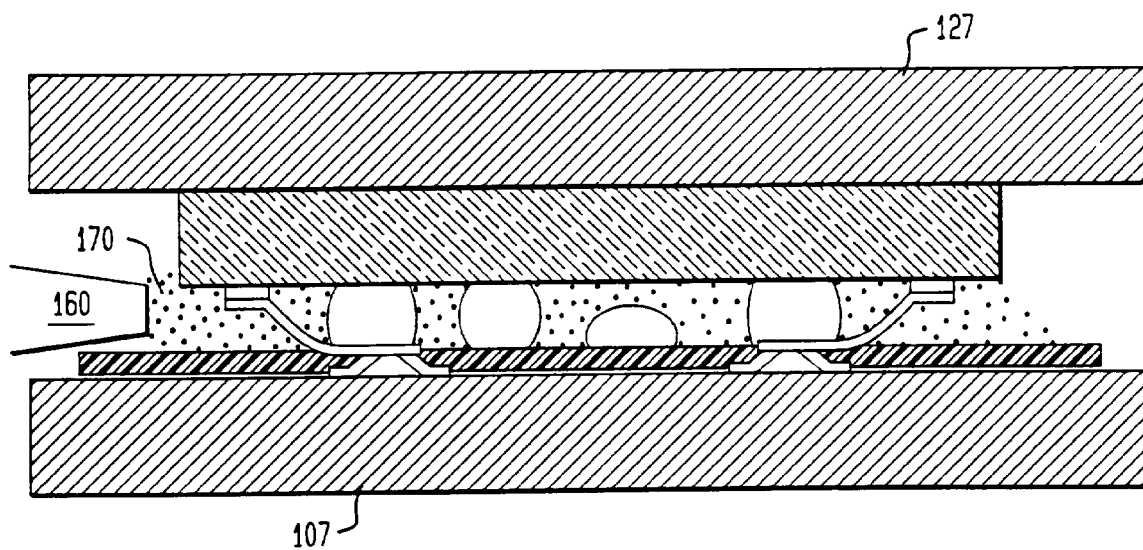


FIG. 2



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FIG. 3A

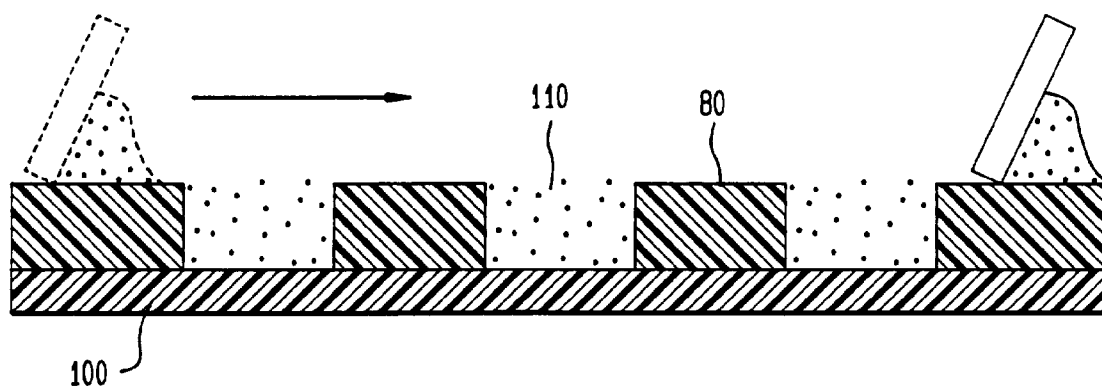
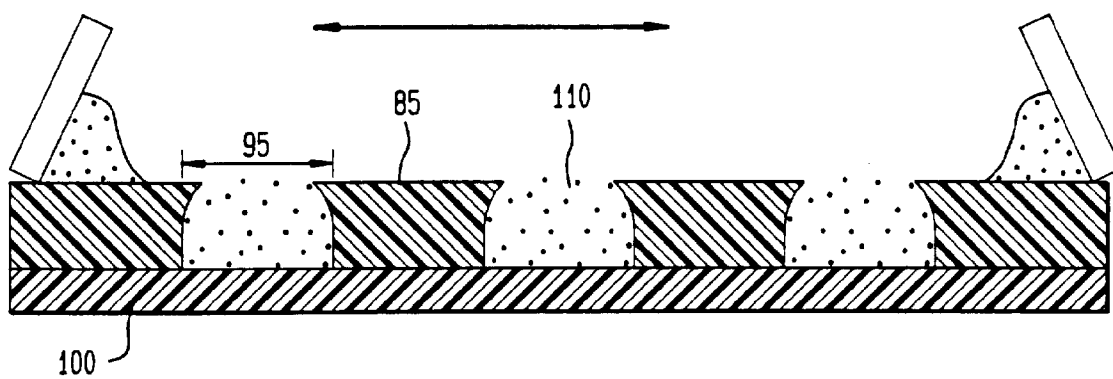


FIG. 3B



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FIG. 4A

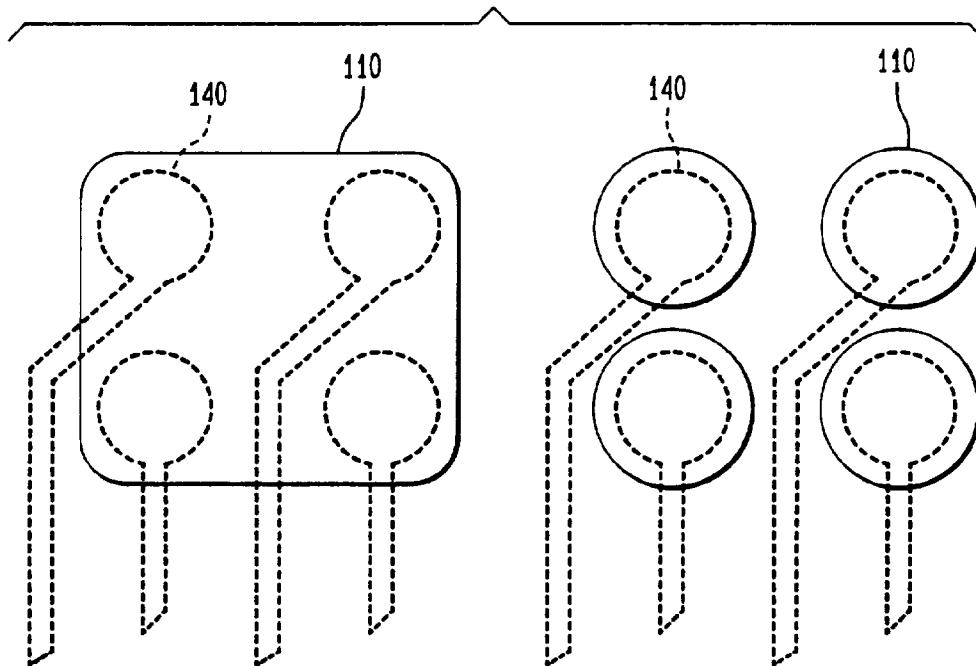
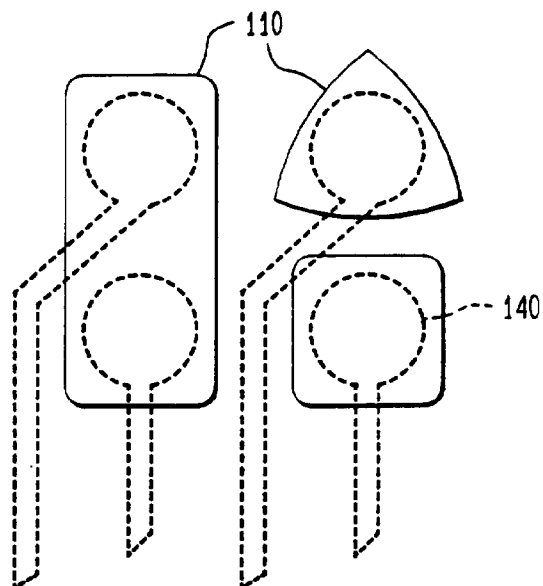
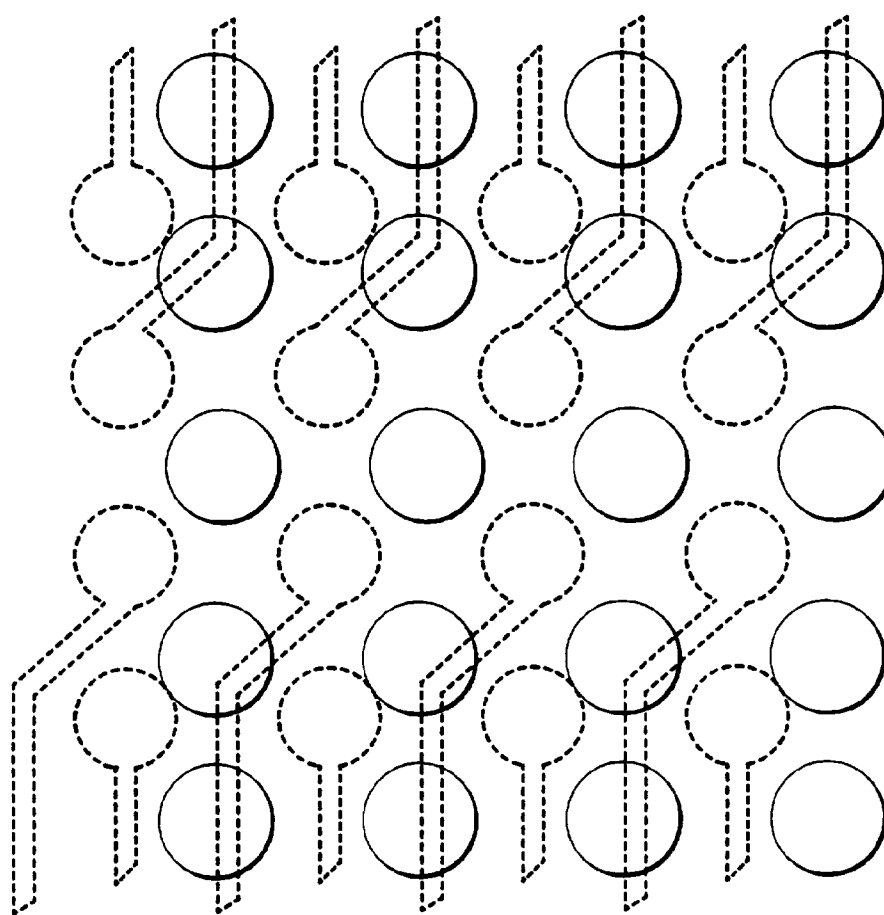


FIG. 4B



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FIG. 4C





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FIG. 5A

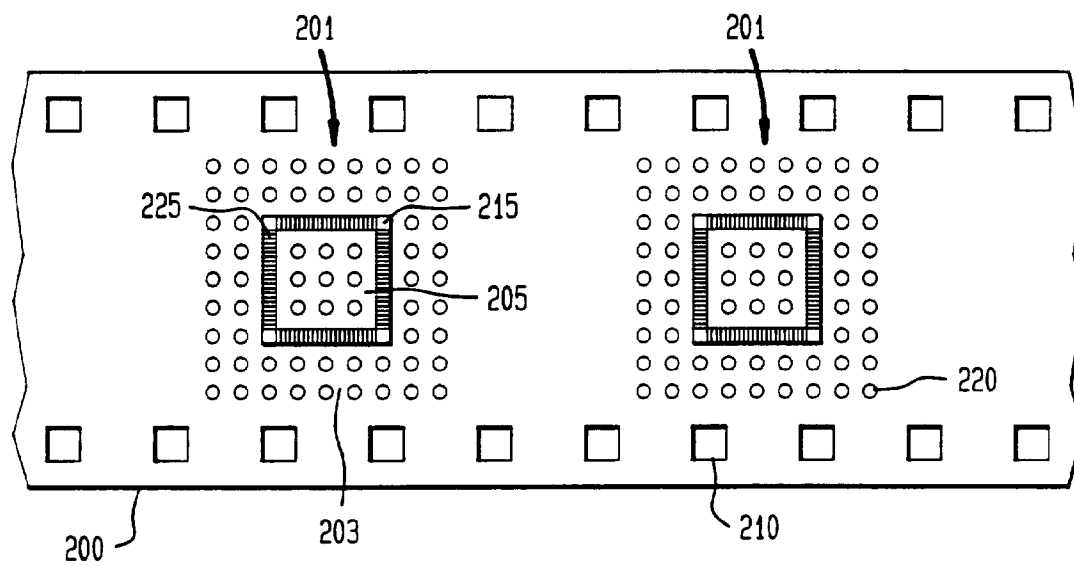
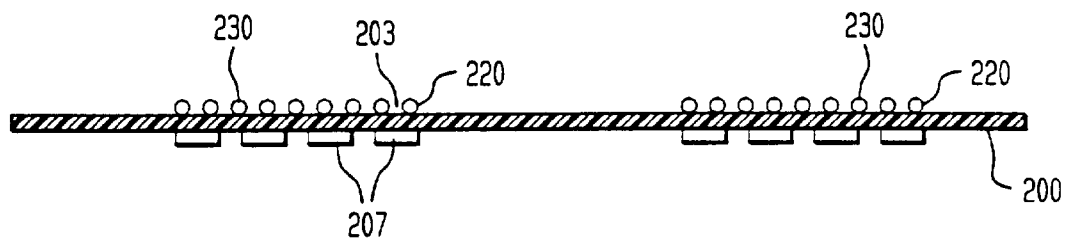


FIG. 5B



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FIG. 5C

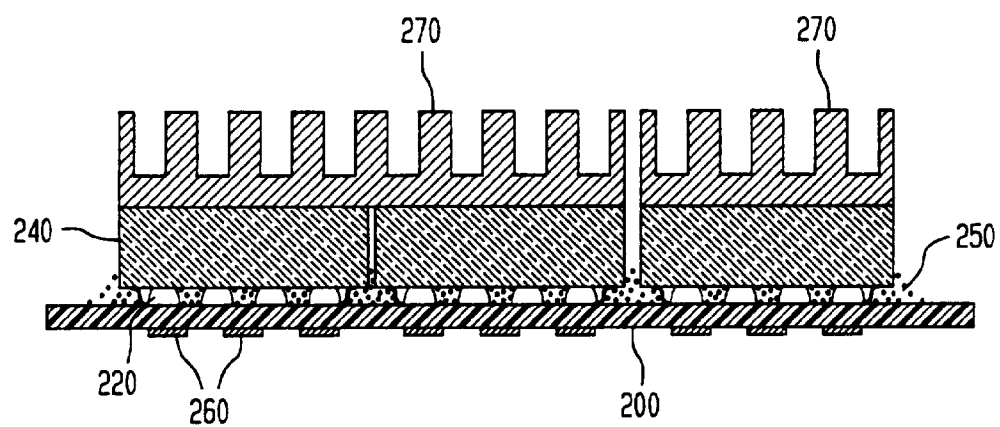
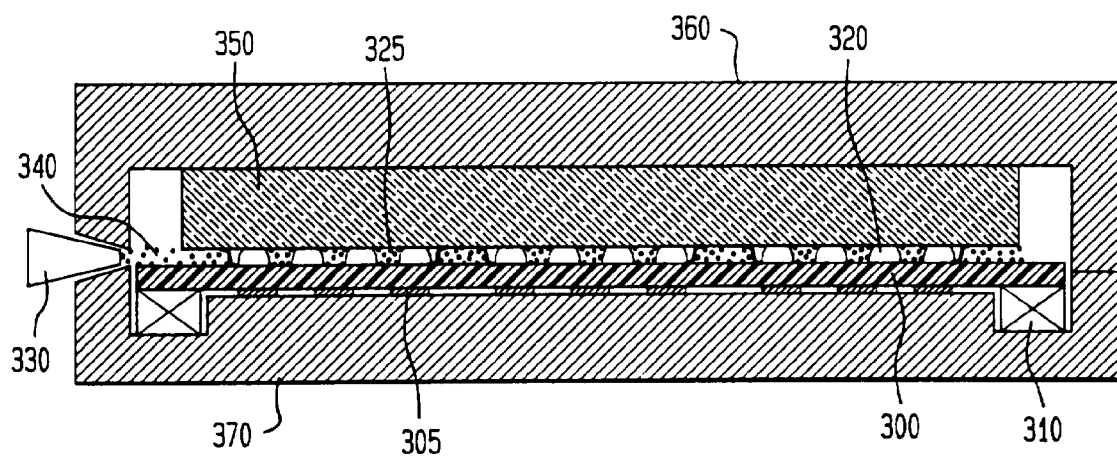


FIG. 6



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FIG. 7

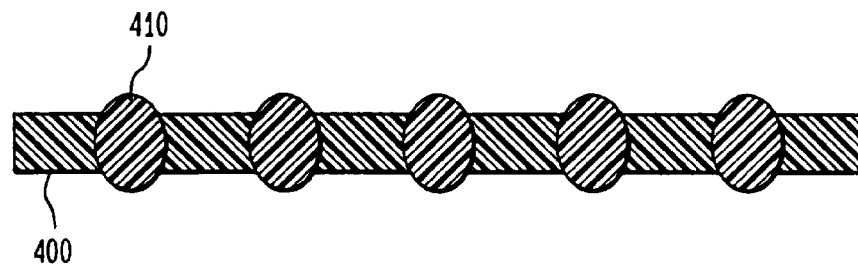
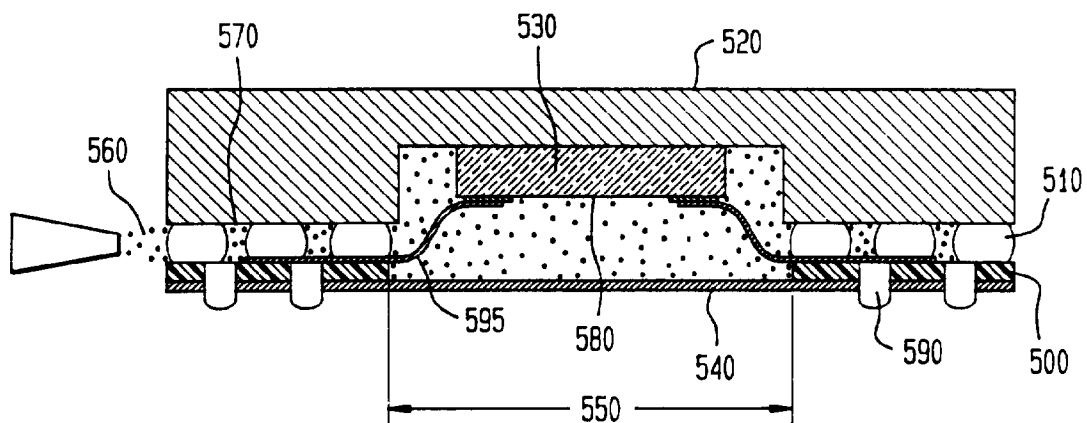


FIG. 8



## INTERNATIONAL SEARCH REPORT

 International application No.  
PCT/US95/11933
**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) : H05K 1/02, 1/11, 3/30; H01L 21/60; H01R 9/09, 4/58

US CL : Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

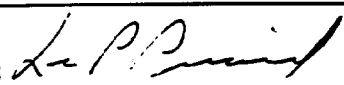
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 5,346,861 (KHANDROS ET AL.) 13 SEPTEMBER 1994, See Figure 2.	34-41
Y	US, A, 5,346,861 (KHANDROS ET AL.) 13 SEPTEMBER 1994, See columns 15-18.	1-33

☐ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 05 DECEMBER 1995	Date of mailing of the international search report 29 FEB 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DONALD SPARKS  Telephone No. (703) 308-1756

# INTERNATIONAL SEARCH REPORT

International application No.

PCT/US95/11933

## A. CLASSIFICATION OF SUBJECT MATTER:

US CL :

29/841, 855; 156/310; 174/255, 258, 259, 261, 262; 228/179.1, 180.1, 180.21, 180.22; 257/692, 693, 698, 723, 724, 737, 747, 753; 361/760, 769, 771, 772, 773, 774, 776, 779, 784, 787, 789, 790, 803; 437/ 209, 211; 439/66, 68, 69, 83, 91

## B. FIELDS SEARCHED

Minimum documentation searched

Classification System: U.S.

29/841, 855; 156/310; 174/255, 258, 259, 261, 262; 228/179.1, 180.1, 180.21, 180.22; 257/692, 693, 698, 723, 724, 737, 747, 753; 361/760, 769, 771, 772, 773, 774, 776, 779, 784, 787, 789, 790, 803; 437/ 209, 211; 439/66, 68, 69, 83, 91